**April 5th Senior Project Meeting**

**Armstrong Hall 148: 2:00PM – 3:00PM**

**Members in Attendance:** Zach, Dhruvit, Kevin, Whitley, Dr. Pearlstein, and Dr. Hernandez

* Zach
  + Last Week
    - Set up final report and presentation
    - Added comments to code
    - Fixed chip output
    - Passed sine, triangular, and square wave through FPGA
    - Started a testing document for FPGA
  + This Week
    - Work on reset warning
    - Further testing of FPGA (maybe with filtering and I2C)
  + Questions
    - VDDIO on PSoC? 🡪 Should be fixed now
* Dhruvit
  + Last Week
    - Made some changes to register.v, filter\_mux.v, filter\_round\_truncate.v
    - Created a new testbench that does not use I2C
    - Worked with EDA tools
    - Worked on FPGA warning
  + This Week
    - Create different filter coefficient combinations to test on FPGA
    - Continue working with physical design of a chip
* Kevin
  + Last Week
    - Testing of chip.v
    - Worked with EDA tools
  + This Week
    - Continue working with physical design of a chip
* Whitley
  + Last Week
    - Worked on I2C PSoC program
  + This Week
    - Finish I2C PSoC program
    - Test I2C PSoC program on FPGA
* Julie
  + Last Week
    - Worked with EDA tools
  + This Week
    - Continue working with physical design of a chip